

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re PATENT APPLICATION Of:

Applicant: Seiji ANDOH)

Serial No.: 09/376,063)

Filed: August 17, 1999)

For: PACKAGE STRUCTURE FOR A)
SEMICONDUCTOR DEVICE)

Art Unit: 2835)

Examiner: M. Datskovskiy)

Attorney Ref. : OKI 226)

APPEAL BRIEF

August 9, 2005

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450
Mail Stop Appeal Brief - Patents

Sir:

INTRODUCTION

This is an Appeal to the Board of Patent Appeals and Interferences from the decision, in the Office Action dated March 22, 2005, finally rejecting claims 20, 22, 24-29 and 31 of the above-referenced application. A Notice of Appeal was timely filed with the applicable fee on June 9, 2005.

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(i) REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Oki Electric Industry Co., Ltd.

(ii) RELATED APPEALS AND INTERFERENCES

A first Notice of Appeal was filed on September 26, 2001 in response to an earlier final rejection, and subsequently supported by an Appeal Brief filed November 26, 2001. As a result of the Appeal, the finality of that action was withdrawn and the prosecution of the application was reopened.

Another Notice of Appeal was filed on February 23, 2004, and subsequently supported by an Appeal Brief filed April 23, 2004 (refiled with minor corrections on June 9, 2004) and a Reply Brief filed September 10, 2004. This second Appeal was effectively withdrawn by the filing of a Request for Continued Examination on February 22, 2005, so that the Examiner might consider an addition Japanese patent reference submitted by the Appellant by way of an Information Disclosure Statement. Thus the first and second appeals were both terminated without the Board having had an opportunity to consider the merits of the Appellant's case.

To the best of the knowledge and belief of the undersigned attorney, there are no other prior or pending appeals, interferences, or judicial proceedings which may be related to, directly affect or be directly affected by, or have a bearing on the Board's decision in the present appeal.

(iii) STATUS OF CLAIMS

Claims 20, 22, 24-29 and 31 are pending in this application. Each of claims 20, 22, 24-29 and 31 stands finally rejected and is under appeal.

(iv) STATUS OF AMENDMENTS

Amendments were filed in this application on July 20, 2000, December 11, 2000, June 5, 2001, November 26, 2001, May 13, 2002, August 26, 2002 and March 6, 2003. All of these previously filed amendments have been entered.

A further Amendment was filed with the Notice of Appeal of June 9, 2005, in order to place the claims in better form for consideration on appeal. In an Office communication dated June 22, 2005, the Examiner acknowledged the Notice of Appeal and indicated that the Amendment filed on June 9, 2005 is entered for the purpose of Appeal. A subsequent Advisory Action dated July 11, 2005 confirmed entry of the Amendment for the purposes of appeal, and maintained the finality of the rejection of claims 20, 22, 24-29 and 31.

(v) SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a package structure for a semiconductor device that has radiation solder bumps and connection solder bumps on the back surface for surface mounting the semiconductor device to a printed circuit board. The inventive semiconductor device, as recited in claim 20 and with reference to Figures 1 and 2 of the application, includes:

- a substrate 11a having a main surface and a back surface, the back surface

having a central area, a distinct intermediate area in which no bumps are disposed, surrounding the central area, and a peripheral area surrounding the intermediate area;

- a semiconductor chip disposed on the main surface;
- a first bump unit 13 disposed in the central area of the back surface; and
- a second bump unit 14 disposed in the peripheral area of the back surface.

The first bump unit located in the central area of the substrate 11a includes a plurality of bumps that are spaced a first distance apart from each other and radiate heat from the semiconductor device to the surface to which the device is mounted (see, for example, page 4, lines 20-21). The second bump unit includes a plurality of bumps that are spaced a second distance apart from each other, the second distance being greater than the first distance between the bumps in first bump unit, and the second bump unit transmits signals to and from the semiconductor device to the printed circuit board to which it is mounted (see, for example, page 4, lines 21-26). In the first bump unit, bumps are spaced close together to achieve an improved coefficient of thermal conductivity between the semiconductor device and the surface on which it is mounted (see, for example, page 5, lines 16-22). Because the first unit of bumps carry no electrical signals, there is no concern that solder bridges may form between the closely spaced bumps of the first bump unit when the bumps are reflowed during the process of surface mounting the semiconductor device. On the other hand, the bumps of the second bump unit carry signals to and from the semiconductor device and are spaced further apart than those in the first bump unit so that short-circuits caused by solder bridges between the bumps of the second bump unit, formed during the mounting process, will not occur (see, for

example, page 5, lines 10-15). For example, the diameter of the radiation bumps 13 and connection bumps 14 is 0.75 mm, the distance between the radiation bumps 13 is 1.00 mm and the distance between the connection bumps is 1.27 mm (page 5, lines 23-26). Preferably, the plurality of bumps included in the first bump unit and the second bump unit are spherical in shape.

In the present invention as claimed, the second distance (i.e., the distance between the connection bumps 14) is less than a third distance between the central area and the peripheral area on the back surface of the substrate 11a. In other words, as recited in claim 22, the width of the intermediate area between the central area and the peripheral area, is greater than the second distance.

To assure an adequate number individual signal connections for the semiconductor device, the plurality of bumps included in the second bump unit is preferably greater in quantity than the plurality of bumps included in the first bump unit (see, for example, page 4, lines 23-26).

In another aspect of the invention, as recited in claims 26 and 28, and with reference to Figures 3 and 4 of the application, the plurality of connection bumps 14 are spaced at a distance sufficient to assure that when heat treatment is applied causing the bumps of the first and second bump units to melt, the connection bumps 14 remain apart from each other and make individual connections to the connection pads 22 on the printed circuit board 20 (see, for example, page 5, lines 10-15). On the other hand, the radiation bumps 13 are sufficiently close to each other that upon application of the heat treatment to the device, they melt and become fused to each other as a unitary body 30 in contact with the radiation pads 21 on the printed circuit board 20 (see, for example, page

5, lines 16-22). As recited in claim 31, the distance between the radiation bumps 13 in the first bump unit is preferably about 1 to 1.4 times their diameter, while the distance between the connection bumps 14 in the second bump unit is preferably about 1.6 to 1.7 times their diameter (see, for example, page 5, lines 26 through page 6, line 1). As recited in claims 27 and 29, the bumps of the first and second bump units are preferably formed of solder (see, for example, page 4, lines 17-19).

(vi) GROUND OF REJECTION TO BE REVIEWED ON APPEAL

Claims 20, 22, 24-29 and 31 stand rejected under 35 U.S.C. §103(a) as being obvious over Bond et al., US Patent No. 5,642,261. Claims 20, 22, 24-29 and 31 are set forth in the claims appendix to this Brief in their currently amended form. Claim language added to claims 26 and 28 by the Amendment file June 9, 2005, and entered for the purposes of appeal, is highlighted.

(vii) ARGUMENT

Appellant respectfully traverses the rejection based on the prior art applied against the claims now pending on appeal. As discussed below, it is respectfully submitted that the Examiner has not met the burden of proof in establishing that the appealed claims are obvious. It is further respectfully submitted that the rejection of the pending claims fails to provide the required factual basis or even a reasonable rationale for the rejection, and fails to apply art that teaches or suggests the claimed invention.

The Rejection for Obviousness Over Bond et al.

The initial burden of establishing a basis for denying patentability to a claimed invention rests upon the examiner. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Thorpe, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985); In re Piasecki, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984).

In rejecting claims under 35 U.S.C. 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). It also is incumbent upon the Examiner to provide a basis in fact and/or cogent technical reasoning to support the conclusion that one having ordinary skill in the art would have been motivated to combine references to arrive at a claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988). In so doing, the Examiner is required to make the factual determinations set forth in Graham v. John Deere Co. of Kansas City, 383 U.S. 1, 148 USPQ 459 (1966), and to provide a reason why one having ordinary skill in the art would have been led to modify the prior art reference to arrive at the claimed invention. Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985). Such a reason must stem from some teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.d 281, 227 USPQ 657 (Fed. Cir. 1985); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983). Inherency requires certainty, not

speculation. In re Rijckaert, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); W. L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); In re Oelrich, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); In re Wilding, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). Objective evidence must be relied upon to defeat the patentability of the claimed invention. Ex parte Natale, 11 USPQ2d 1222 (BPAI 1988). Teaching away from the claimed invention by the prior art is a per se demonstration of lack of prima facie obviousness. In re Dow Chemical Co., 837 F.2d 469, 5 USPQ2d 1529 (Fed. Cir. 1988), In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), In re Nielson, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987)

In determining obviousness, the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed. Hartness Int'l, Inc. v. Simplimatic Eng'g Co., 819 F.2d 1100, 2 USPQ2d 1826 (Fed. Cir. 1987). It is impermissible to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. In re Wesslau, 353 F.2d 238, 147 USPQ 391 (CCPA 1951). Piecemeal reconstruction of prior art patents is improper, In re Kamm, 452 F.2d 1052, 172 USPQ 298 (CCPA 1972). The Examiner must give adequate consideration to the particular problems and solution addressed by the claimed invention. Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); In re Rothermel, 276 F.2d 393, 125 USPQ 328 (CCPA 1960).

The fact that the prior art could be modified so as to result in the combination defined by the claims does not make the modification obvious unless the prior art suggests the desirability of the modification. In re Deminski, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986). The test is what the combined teachings would have suggested to those of ordinary skill in the art. In re Keller, 642 F.2d 413, 208 USPQ 817 (CCPA 1981). Simplicity and hindsight are not proper criteria for resolving obviousness, In re Warner, supra. The proper approach to the issue of obviousness is whether the hypothetical person of ordinary skill in the art, familiar with the references, would have found it obvious to make a structure corresponding to what is claimed. In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983). Hindsight obviousness after the invention has been made is not the test. In re Carroll, 601 F.2d 1184, 202 USPQ 571 (CCPA 1979). The reference, viewed by itself and not in retrospect, must suggest doing what applicant has done. In re Shaffer, 229 F.2d 476, 108 USPQ 326 (CCPA 1956); In re Skoll, 523 F.2d 1392, 187 USPQ 481 (CCPA 1975).

The issue is not whether it is within the skill of the artisan to make the proposed modification but, rather, whether a person of ordinary skill in the art, upon consideration of the references, would have found it obvious to do so. The fact that the prior art could be modified so as to result in the combination defined by the claims would not have made the modification obvious unless the prior art suggests the desirability of the modification. See In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984), In re Deminski, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986), In re Keller, supra. See In re Laskowski, F.2d., 10 USPQ2d 1397 (CAFC 1989). References are not properly combinable or modifiable if their

intended purpose or function is destroyed by the combination or modification. See In re Gordon, *supra*.

Obviousness does not require absolute predictability but a reasonable expectation of success is necessary. *In re Clinton*, 527 F.2d 1226, 188 USPQ 365 (CCPA 1976), *Amgen, Inc. v. Chugai Pharmaceutical Co. Ltd.*, 927 f.2d 1200, 18 USPQ2d 1016 (Fed. Cir. 1991). A prior art suggestion for virtually endless experimentation is not a case of *prima facie* obviousness. *In re Dow Chemical Co.*, 837 F.2d 469, 5 USPQ2d 1529 (Fed. Cir. 1989).

The Bond et al. patent ("Bond") describes a ball grid array (BGA) integrated circuit package that provides a path of high thermal conductivity for an encapsulated integrated circuit chip. The package utilizes a substrate through which an opening has been formed to receive a thermally conductive slug, made of a material such as copper. The integrated circuit chip is mounted to one surface of the slug, and the opposite surface of the slug is exposed at the underside of the substrate. The chip is wire bonded to the substrate and connected in the conventional manner through the substrate to lands on the underside of the substrate outside the periphery of the slug. Solder balls are attached to the underside of the substrate and of the slug in ball-grid-array fashion, for mounting to a circuit board. Upon mounting to the circuit board, a path of high thermal conductivity is formed between the chip and the circuit board, through the slug and the solder balls. According to one of the disclosed embodiments, the slug extends below the underside of the substrate and has a solder mask with larger apertures than those used for the electrical connections to the substrate, so that when solder balls with equivalent volumes are used to connect to the circuit board, broader conductive leads are formed under the slug for enhanced conductivity.

In the Final Office Action, the Examiner relies upon Bond to teach the features of the semiconductor device claimed in the present invention. Specifically, the Examiner points to Bond as teaching a semiconductor device 8 (Figures 1-6), comprising a semiconductor substrate 14 having a main surface and a back surface, wherein the back surface has a central area, a distinct intermediate area surrounding the central area and a peripheral area surrounding the intermediate area; a semiconductor chip formed on the main surface; a first bump unit formed of solder bumps 18 disposed a first distance apart from each other, and located in the distinct area beneath a thermally conducted slab 12 in the central area of the back surface, wherein the first bump unit radiates heat from said semiconductor device; a second bump formed of solder bumps 18 disposed a second distance apart from each other located in the peripheral area of the back surface, wherein the second bump unit transmits signals, wherein the second bump unit is greater in quantity of solder balls than the first bump unit, and the solder balls are spherical in shape. With regard to the claim requirements that the second distance is greater than the first distance, that the second distance is less than a width of the intermediate area, and that the bumps of first (central) bump unit are located sufficiently close to each other that upon the application of heat treatment to the device, they will fuse into a unitary body (claims 20, 22, 24-29), and with respect to the requirement that the first distance is about 1 to 1.4 times the diameter of bumps of the first bump unit and the second distance is about 1.6 to 1.7 times the diameter of the bumps of the second bump unit (claims 31), the Examiner asserts it would have been obvious to one skilled in the art at the time the invention was made to employ a distinct intermediate area between the first and second groups of solder balls, the second distance being less than the width of the intermediate

area, and to locate the bumps of the first bump unit so close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit would be fused into us a unitary body, or to make the first distance about 1 to 1.4 times the diameter of the bumps of the first bump unit, and the second distance about 1.6 to 1.7 times the diameter of the bumps of the second bump in the devise by Bond in order to avoid shorting between thermal and signal solder balls, or to melt the thermal solder balls into a unitary body, while applying heat. The Examiner argues that such a modification of Bond would have involved a mere change in the sizes of components or a mere change in the ranges of sizes, and that such changes are generally recognized as being within the level of ordinary skill in the art. The Examiner also argues that the changes in distance and size would have been obvious to one having ordinary skill in the art at the time the invention was made since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or workable ranges involves only routine skill in the art.

Independent Claim 20 and Dependent Claims 22, 24-25 and 31

The Appellant disagrees with the Examiner's assertion that the claimed relationships between the first and second distances, and between the second distance and the width of the intermediate area, are merely the discovery of "the optimum or workable ranges" that involve "only routine skill in the art" that would render the claims obvious to one of ordinary skill. Rather, these features clearly patentably distinguish the independent claims over the teachings of the applied prior art. While, Bond generally discloses the presence of central and peripheral areas of solder bumps, distinguished by their respective thermal and signal transfer functions, it fails to disclose any requirement

regarding the respective spacings within or between the bump units. For example, Figures 1, 3, 4 and 6, which show the various embodiments in cross section, do not disclose any consistent pattern of spacing between bumps in the central and peripheral areas. In fact, it appears from the figures that the spacing between bumps is generally the same in both areas.

Further, it is submitted that Bond lacks any disclosure of a distinct intermediate area, which is devoid of bumps and has a width greater than the distance between the bumps in the peripheral area, as the claims require. The scope of the limitation “a distinct intermediate area in which no bumps are disposed,” recited in the present claims, should, in this case, be construed with reference to the specification, where a distinct intermediate area having no bumps is shown, for example, in Figures 1-3. See In re Barr, 44 F.2d 588, 170 USPQ 330 (CCPA 1971). In contrast, Bond discloses no such clear gap between the central and peripheral areas. The only general limitation taught by Bond is that the peripheral array of signal bumps must be located outside the dimensional profile of the thermal conductive slug.

Independent Claims 26 and 28 and Dependent Claims 27 and 29

In the claimed invention, “the first and second distances are set such that upon application of a heat treatment to the device, the bumps of the first bump unit melt so as to become connected and fuse to each other as a unitary body and the bumps of the second bump unit melt and remain apart from each other.” In Bond, on the other hand, the relative distances between bumps in the central and peripheral areas are not of principal concern because the degree to which the solder balls spread in the central area, when the device is heated to mount it to a circuit board, is determined by the apertures 83

in solder mask 81 positioned on the bottom of conductive slug 72 (see Figures 5 and 6). Using solder balls in the central and peripheral areas having the same equivalent volume, the result, in the preferred embodiment in Bond, is that the solder leads 80' in the central area under the slug, after reflowing the solder balls, will have a cross-sectional area that, on average, is approximate twice that of the leads 78' in the peripheral area (column 7, line 66, through column 8, line 2). Bond fails to teach or suggest in any way that "the bumps of the second bump unit melt so as to become connected and fuse to each other as a unitary body," as presently claimed. Rather, Bond clearly teaches away from the present invention by using a solder mask to keep the central solder leads separate. Hence, it is submitted that the prior art relied upon by the Examiner provides no motivation to modify the prior art to arrive at the claimed invention. The difference between the claimed invention and Bond is not a matter of degree, as the Examiner asserts, but rather one of kind. The Appellant believes that the Examiner has simply not met the burden of establishing a clearly reasoned basis for denying patentability.

In the Response to Arguments section of the Final Office Action, the Examiner begins by observing that the Appellant claims a semiconductor device having a plurality of separate solder bumps grouped distinctly in the signal peripheral area and in the heat transferring central area. The Examiner notes, in particular, that the appellant does not claim a unitary heat transferring body made of the group of solder bumps and heat transfer area as part of the claimed structure. Instead, the solder bumps and heat transfer area are claimed as being placed close enough to be melted together upon application of a heat treatment (see, for example, claim 26). The Examiner asserts that none of the important aspects of this technological process, such as size of the solder

bumps, type of solder, temperature and length of the heat treatment, has been claimed or explained in the specification.

The Appellant respectfully disagrees. The range of diameters and spacing of the solder bumps in the heat transfer area appropriate for forming a unitary solder mass is in fact described in the application at page 5, lines 23-28. This range is expressly reflected in claim 31.

More significantly, the Examiner argues at a later point in his rebuttal that the technology of solder ball connections is well-known in the art, and it would be obvious that melting the heat transmitting balls together could be achieved by manipulating the sizes of the balls and/or the distances between them. The Examiner also later quotes with approval a statement made by the Appellant in a previous communication that "in this case, a person of ordinary skill in the art could readily determine what spacing, or range of spacings, of the bumps in the first bump unit would be sufficiently close such that the bumps would fuse into a unitary body upon application of the heat treatment." These statements by the Examiner are clearly inconsistent with his initial assertion that Appellant has not provided sufficient information in the application to support the claimed structure, i.e., bumps in the first bump unit that are sufficiently close to each other that upon application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body.

The Examiner points in his rebuttal arguments to Bond as teaching a semiconductor device 8, Figures 1-6, also having two distinct groups of separate solder bumps 18: one in the signal, peripheral area and another in the heat transferring, central area. The Examiner asserts that in discussing the figures of the Bond reference,

Appellant has omitted Figure 2, which clearly shows solder balls 18 located in the central, heat transfer area without any distance between them, which makes it obvious enough, according to the Examiner, to conclude that upon applying heat they would definitely melted together. The Examiner also notes that on the same Figure 2, the signal solder bumps are shown located distinctly apart from the central group of bumps, undoubtedly construing Figure 2 to show the claimed feature "a distinct intermediate area in which no bumps are disposed."

The Examiner places great reliance on Figure 2 of Bond. Figure 2 is an overall plan view showing the semiconductor device 8 already attached to system circuit board 20 (Bond column 3, lines 49-51). However, it is known that patent drawings are often lacking in detail and often not to scale, and Appellant believes it is unwarranted to conclude on the basis of Figure 2 alone that the bumps in the central area under conductive slab 12 are very close or even touching each other. Figure 1 is a cross-section of the same embodiment along sectional line 1-1 (column 3, lines 46-49) in the immediate vicinity of the semiconductor device 8, and reveals far more detail than Figure 2. Figure 1 shows that solder balls 18 under the conductive slab 12 are not in contact with each other, and in fact, do not appear to be any closer to each other than the solder balls in the peripheral area. Perusal of the other figures in Bond also fails to disclose any embodiment in which the solder balls in the central area are touching each other or fuse together after the reflow process (see particularly Figure 6). Contrary to the Examiner's position, it is submitted that when the reference is considered as a whole, it is not obvious that the solder balls under the central area of the semiconductor device in Bond would fuse together when heated to form a unitary mass.

In his rebuttal arguments, the Examiner disagrees with Appellant's position that the difference between the claimed invention and Bond is not a matter of degree, but rather one of kind. The Examiner asserts that, on the contrary, both devices are substantially similar semiconductor packages having similar packaging, electronic and cooling designs, such that the difference is not even a matter of degree.

Interestingly, the Examiner admits that Bond does not claim certain relationships between distances between groups of solder balls and the solder balls themselves, apparently referring to limitations in the claims of the present invention that are directed to the relationship among the distance between bumps in the central area, the distance between bumps in the peripheral area, and the distance between the central area and the peripheral area (see, for example, claim 20). Rather, the Examiner relies on his interpretation of Figure 2, discussed above, and on the allegedly well-known technology of solder ball connections which teaches avoiding shorting between solder balls during the reflow (heating) process by manipulating the sizes the sizes of the balls and/or the distance between them. The Examiner argues that it would be obvious to conclude that in the device of Bond an entirely opposite result, i.e. melting the solder balls together, could also be achieved by manipulating sizes of the heat transmitting solder balls and/or the distances between them. In the Examiner's view, that is what was done in Bond in order to prevent the signal solder bumps for shorting between themselves and with the heat transfer solder bumps.

The Examiner's argument ignores the fact, discussed above, that Bond totally fails to disclose any melting together of the solder bumps in the central area under the conductive slab 12 during the reflow process used to mount the semiconductor device 18 to the main circuit board 20. This feature is neither referred to in the text nor shown in the figures. In

fact, Bond teaches away for any such fusion of the solder balls in the central area during reflow. Figure 6 shows that Bond employs a solder mask 81 (Figure 5) under conductive slug 72 to define and limit the shape of the resulting solder leads 80' (column 7, lines 35-39).

Other prior art that has been previously applied in this case by the Examiner is similarly lacking in any teaching or suggestion regarding this key feature. For example, the Katchmar reference (U.S. Patent No. 6,194,782 B1) discloses in one embodiment (Figure 5), the use of solder balls arranged in close proximity to each other under the semiconductor chip (die) 18 in the central area. However, Katchmar fails to teach or suggest that the solder balls in this embodiment are melted and fused together to form a unitary body as a result of heat treatment during the mounting process, as claims 26 and 28 require. Katchmar also discloses in another embodiment (Figure 4) the use of a single central solder mass 26 that bonds during the reflow process to both the solderable pad 32 on the bottom surface 16 of the package substrate 12 and the solderable pad 34 on the top surface 30 of the printed circuit 28. The first-mentioned embodiment is fabricated with solder balls under the central area that retain their individual identity after heat treatment, and the second-mentioned embodiment starts with a single central solder mass that similarly retains its character after heat treatment. There is simply no suggestion in Katchmar to modify the first-mentioned embodiment to replicate the results of the second mentioned embodiment.

Under applicable law, as cited above, the issue is not whether it is within the skill of the artisan to make the proposed modification but, rather, whether a person of ordinary skill in the art, upon consideration of the references, would have found it obvious to do so. The

fact that the prior art could be modified so as to result in the combination defined by the claims would not have made the modification obvious unless the prior art suggests the desirability of the modification. It is the Appellant's position that neither Bond nor any of the other prior art relied upon by the Examiner suggest the desirability of the feature of having bumps in the first bump unit that are sufficiently close to each other that upon application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body.

CONCLUSION

In summary, it is respectfully submitted that the Examiner has (i) failed to establish a prima facie case for the rejection, (ii) failed to apply art which teaches or suggests, the claimed invention, and (iii) has applied art in a manner inconsistent with its teachings. The applied art does not provide any teaching, or suggestion within its teachings, which would lead to the features or advantages of the instant invention discussed above, and that for at least these reasons the appealed claims patentably define over the art.

Thus, it is submitted that the rejection of claims 20, 22, 24-29 and 31 under 35 U.S.C. §103(a) as obvious over Bond et al., U.S. Patent No. 5,642,261, is in error and reversal is clearly in order and is courteously solicited.

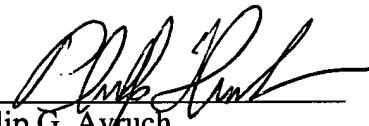
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The Appeal Brief fee of \$500 is included in a remittance that is being submitted concurrently. Should this remittance be accidentally missing or insufficient in amount, or should additional fees be required, please charge any deficiency to our Deposit Account No. 18-0002 and notify the undersigned attorney accordingly.

Respectfully submitted,

August 9, 2005

Date



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(viii) Claims Appendix

The following claims are under appeal:

20. A semiconductor device, comprising:
- a substrate having a main surface and a back surface,
 - wherein said back surface has a central area, a distinct intermediate area in which no bumps are disposed, surrounding said central area, and a peripheral area surrounding said intermediate area;
 - a semiconductor chip disposed on said main surface;
 - a first bump unit disposed in said central area of said back surface,
 - wherein said first bump unit includes a plurality of bumps that are disposed a first distance apart from each other, and
 - wherein said first bump unit radiates heat from said semiconductor device;
 - and
 - a second bump unit formed in said peripheral area of said back surface,
 - wherein said second bump unit includes a plurality of bumps that are disposed a second distance apart from each other, said second distance is greater than said first distance, and said second distance is less than a third distance between said central area and said peripheral area, and
 - wherein said second bump unit transmits signals.
22. The semiconductor device in accordance with Claim 20, wherein a width of said intermediate area of said back surface is greater than said second distance.

24. The semiconductor device in accordance with Claim 22, wherein said plurality of bumps included in said second bump unit is greater in quantity than said plurality of bumps included in said first bump unit.

25. The semiconductor device in accordance with Claim 24, wherein said plurality of bumps included in said first bump unit and said second bump unit are spherical in shape.

26. A semiconductor device, comprising:

a substrate having a main surface and a back surface, the back surface having a central area, a distinct intermediate area in which no bumps are disposed, surrounding the central area, and a peripheral area surrounding the intermediate area;

a semiconductor chip disposed on the main surface;

a first bump unit disposed in the central area of the back surface to radiate heat from the semiconductor device, the first bump unit including a plurality of bumps disposed a first distance apart from each other; and

a second bump unit formed in the peripheral area of the back surface for transmitting signals, the second bump unit including a plurality of bumps disposed a second distance apart from each other, the second distance being greater than the first distance and less than a third distance between the central area and the peripheral area,

wherein the first and second distances are set such that upon application of a heat treatment to the device for the purpose of mounting the device to a circuit board, the bumps of the first bump unit melt so as to become connected and fuse to each other as a

unitary body and the bumps of the second bump unit melt and remain apart from each other.

27. The semiconductor device according to claim 26, wherein the bumps of the first and second bump units are formed of solder.

28. A semiconductor device, comprising:

a substrate having a main surface and a back surface, the back surface having a central area, a distinct intermediate area in which no bumps are disposed, surrounding the central area, and a peripheral area surrounding the intermediate area;

a semiconductor chip disposed on the main surface;

a first bump unit disposed in the central area of the back surface to radiate heat from the semiconductor device, the first bump unit including a plurality of bumps disposed a first distance apart from each other; and

a second bump unit formed in the peripheral area of the back surface for transmitting signals, the second bump unit including a plurality of bumps disposed a second distance apart from each other sufficient to assure that upon application of a heat treatment to the device for the purpose of mounting the device to a circuit board, causing the bumps of the first and second bump units to melt, the bumps of the second bump unit remain apart from each other, the second distance being greater than the first distance and less than a width of the intermediate area;

wherein the bumps of the first bump unit are sufficiently close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body.

29. The semiconductor device according to claim 26, wherein the bumps of the first and second bump units are formed of solder.

31. The semiconductor device according to claim 25, wherein the first distance is about 1 to 1.4 times the diameter of the bumps of the first bump unit, and the second distance is about 1.6 to 1.7 times the diameter of the bumps of the second bump unit.

(ix) Evidence Appendix

No new evidence is being submitted with this Brief.

(x) Related Proceedings Appendix

In view of section (ii) of this Brief, no copies of decisions are appended.